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TITLE: CLAMPING AND DE-CLAMPING SEMICONDUCTOR WAFERS
ON AN ELECTROSTATIC CHUCK USING WAFER INERTIAL
CONFINEMENT BY APPLYING A SINGLE-PHASE SQUARE
WAVE AC CLAMPING VOLTAGE

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RELATED APPLICATIONS

This application is related to U.S. Application Serial No. _____,
filed on August 18, 2003, attorney docket No. 03-IMP-056, entitled, "MEMS
Based Multi-Polar Electrostatic Chuck" which is incorporated herein by reference,

10   and U.S. Application Serial No. _____, filed on _____, attorney
docket No. 03-IMP-002, entitled, "Clamping and De-clamping Semiconductor
Wafers on a J-R Electrostatic Chuck Having a Micromachined Surface by Using
Force Delay in Applying a Single-Phase Square Wave AC Clamping Voltage".

15   ## FIELD OF THE INVENTION

The present invention relates generally to semiconductor processing
systems, and more specifically to a method for clamping a wafer to an
electrostatic chuck by applying a single-phase square-wave AC clamping
voltage.

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BACKGROUND OF THE INVENTION

Electrostatic chucks (ESCs) have been utilized in plasma-based or
vacuum-based semiconductor processes such as etching, CVD, and ion
implantation, etc. for a long time. Capabilities of the ESCs, including non-edge

25   exclusion and wafer temperature control, have proven to be quite valuable in
processing semiconductor substrates or wafers, such as silicon wafers. A typical
ESC, for example, comprises a dielectric layer positioned over a conductive
electrode, wherein the semiconductor wafer is placed on a surface of the ESC
(e.g., the wafer is place on a surface of the dielectric layer). During

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semiconductor processing (*e.g.,* plasma processing), a clamping voltage is typically applied between the wafer and the electrode, wherein the wafer is clamped against the chuck surface by electrostatic forces. Furthermore, the wafer can be cooled by introducing a gas, such as helium, and applying

5 backpressure between the wafer and dielectric layer. A temperature of the wafer can then be controlled by adjusting the backpressure between the wafer and the dielectric layer.

Declamping or un-sticking the wafer from the chuck surface, however, is a concern in many ESC applications. For example, after the clamping voltage is

10 turned off, the wafer typically "sticks" to the chuck surface for a considerable amount of time, wherein the wafer cannot be removed by typical wafer lifting mechanisms (*e.g.,* pins extending through the ESC which are operable to lift the wafer from the surface of the dielectric layer). This wafer declamping problem can reduce the throughput of the process. It is believed that the wafer-

15 declamping problem occurs when residual charges induced by the clamping voltage remain on the dielectric layer or on a surface of the wafer, therein leading to an undesirable electric field and clamping force. According to a charge migration model, residual charges are caused by charge migration and accumulation during clamping, wherein the charges accumulate at the dielectric

20 surface and/or wafer backside (*e.g.,* when the wafer surface comprises an insulating layer).

An *RC* time constant, for example, can be used to characterize the charge/discharge times which correspond to an amount of time typically required to respectively clamp or de-clamp the wafer. This time constant is determined by

25 the product of a volume resistance of the dielectric layer and a gap capacitance between the wafer and dielectric surfaces, *i.e.,*

$$RC = R_{die}C_{gap} = \rho(dielectric)\varepsilon_0\varepsilon_r \frac{d(dielectric)}{gap} \qquad (1)$$

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where R_{die} is the resistance of the dielectric layer, C_{gap} is the capacitance of the gap between the wafer and the chuck surface, $\rho(dielectric)$ is the volume resistivity of the dielectric layer, ε_0 is the free space permittivity, ε_r is the dielectric constant of the gap, $d(dielectric)$ is the thickness of the dielectric layer, and gap is

5   the distance between the dielectric and wafer surfaces. For example, for a typical flat-plate ESC, if we assume that $\rho(dielectric)$ = 10^{15} Ω–cm, ε_0 = 8.85×10^{-14} F/cm, ε_r=1, $d(dielectric)$ = 0.2 mm, and gap = 3 μm, we find RC = 5900 seconds. This is a fairly long charging/discharging time, meaning that if clamping is longer than 5900 seconds, the declamping time will also last approximately

10   5900 seconds.

A variety of techniques have been previously disclosed for reducing wafer de-clamping problems encountered in the use of ESCs. For example, one conventional technique involves applying a reversal voltage before the wafer is removed from the ESC, therein eliminating a residual attractive force. This

15   reversal voltage, however, is typically 1.5 to 2 times higher than the clamping voltage, and the de-clamping time is still typically quite large. Another conventional technique involves providing a low-frequency sinusoidal AC voltage in order to produce sine wave fields of controlled amplitude and phase. Such low-frequency sinusoidal AC voltages, however, typically provide low clamping

20   forces, as well as fairly long residual clamping times.

Other conventional techniques for de-clamping the wafer include determining a value of an opposite polarity DC drive voltage to be applied to the electrodes in order to cancel the holding effects of the residual electrostatic charge, and thus enable a release of the wafer. Typically, however, this

25   technique involves quite complicated timing circuits, and do not appear to be optimized for wafer inertial effects, backpressure from a cooling gas, or an overall RC time constant of the electrostatic chuck.

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Therefore, a need exists in the art for a clamping and declamping system and method which are optimized for wafer inertial effects, as well as for physical and electrical properties of an electrostatic chuck.

5 **SUMMARY OF THE INVENTION**

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an extensive overview of the invention. It is intended to neither identify key or critical elements of the invention nor delineate the scope of the invention. Its

10 purpose is to present some concepts of the invention in a simplified form as a prelude to the more detailed description that is presented later.

Challenges of the prior art are overcome in the present invention by applying a single-phase square-wave AC voltage to an electrostatic chuck (ESC), wherein a polarity of the square-wave voltage, for example, is switched faster

15 than an inertial response time of a semiconductor wafer being clamped. The present invention utilizes a relatively simple and inexpensive apparatus, in comparison with various conventional electrostatic chucks. As opposed to some conventional techniques which attempt to remove a residual charge as quickly as possible, the method and system of the present invention are designed to

20 generally prevent the residual charge from being generated in the first place. The method is referred to as "wafer inertial confinement", and employs a square wave single-phase AC clamping voltage which can be applied to either a uni-polar or a multi-polar electrode ESC. De-clamping time can further be minimized by adjusting a pulse width and a pulse rise-time of the applied voltage.

25 According to one aspect of the present invention, the method is applicable to flat-plate ESCs as well as MEMS-based ESCs, wherein the semiconductor wafer is clamped and de-clamped *via* a wafer inertial confinement mechanism.

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By controlling parameters such as rise-time, pulse width, and pulse repetition frequency (prf) of a single-phase square wave AC signal, the semiconductor wafer can be reliably clamped due, at least in part, to an inertial mass of the wafer during voltage switching. Furthermore, according to another exemplary

5 aspect of the invention, the wafer can be almost instantaneously de-clamped after the clamping voltage is turned off, due at least in part to the pulse width during clamping being short enough to significantly prevent charge migration and accumulation to a dielectric front surface and/or back surface of the wafer.

According to yet another exemplary aspect of the invention, the ESC may

10 comprise electrode patterns of various types, including, for example, a simple uni-polar structure for a plasma-environment system or a simple D-shape bi-polar structure for a vacuum-environment system. Furthermore, the present invention does not require complicated electrode patterns or complex signal timing control electronics.

15 To the accomplishment of the foregoing and related ends, the invention comprises the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative embodiments of the invention. These embodiments are indicative, however, of a few of the various ways in which the principles of the

20 invention may be employed. Other objects, advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

25 Fig. 1 is a system-level block diagram of an exemplary electrostatic chuck according to one aspect of the present invention.

Figs. 2A-2D are graphs illustrating waveforms of clamping voltage, wafer

position, velocity, and acceleration as a function of time for an exemplary classic ESC according to another aspect of the present invention.

Fig. 3 illustrates an exemplary MEMS-based ESC according to still another exemplary aspect of the present invention.

5   Figs. 4A-4D are graphs illustrating waveforms of clamping voltage, wafer position, velocity, and acceleration as a function of time for an exemplary MEMS-based ESC according to another aspect of the present invention.

Fig. 5 illustrates an exemplary method for clamping and declamping a wafer according to another exemplary aspect of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed towards a system and a method for clamping and de-clamping a wafer utilizing an electrostatic chuck (ESC). Accordingly, the present invention will now be described with reference to the

15   drawings, wherein like reference numerals are used to refer to like elements throughout. It should be understood that the description of these aspects are merely illustrative and that they should not be taken in a limiting sense. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It

20   will be evident to one skilled in the art, however, that the present invention may be practiced without these specific details.

The present invention overcomes challenges of the prior art by providing a system and a method for clamping and de-clamping a wafer (e.g., a semiconductor substrate), wherein a predetermined square-wave voltage is

25   applied to the electrostatic chuck, therein selectively clamping the wafer thereto. According to one exemplary aspect of the present invention, the predetermined square-wave voltage is a function of inertial properties of the wafer, electrical

properties of the electrostatic chuck and a backside pressure associated a cooling gas between the wafer and the ESC.

Referring now to the drawings, Fig. 1 illustrates a block diagram of an exemplary clamping system 100, wherein the clamping system comprises an
5   electrostatic chuck 105 for selectively clamping a wafer 110 thereto. A voltage source 115, for example, is operable to selectively provide a voltage potential V to the ESC 105, wherein the voltage potential is operable to selectively electrostatically clamp and de-clamp the wafer 110 to and from a surface 120 of a dielectric layer 125 of the ESC. According to one exemplary aspect of the
10   invention, the voltage source 115 is operable to provide a single-phase square wave AC clamping voltage V to the ESC 105. Providing a single-phase square wave AC clamping voltage V, for example, can minimize a de-clamping time for the wafer 110, wherein a pulse width and pulse rise-time associated with the square wave are operable to control the de-clamping time, as will be discussed
15   *infra*. The system 100, for example, further comprises a gas supply 130 operable to provide a backside gas pressure P (also referred to as the cooling gas backpressure force F_{gas}) to the wafer 110. The gas supply 130, for example, is operable to provide a cooling gas (not shown), such as helium, between the surface 120 of the ESC 105 and the wafer 110. A controller 135, for example, is
20   further operable to control the pressure P of the cooling gas, wherein the control of the pressure is further operable to control an amount of heat transfer between the ESC 105 and the wafer 110. The controller 135, for example, is further operable to control the application of the clamping voltage V by the voltage source 115 (*e.g.,* a power supply) to the ESC 105.

25   Providing a square wave clamping voltage V to the ESC 105 in order to efficiently clamp and de-clamp the wafer 110 comprises overcoming several difficulties. For example, a square-wave clamping voltage V applied to the ESC

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105 is operable to induce an electrostatic clamping force F_{esc} on the wafer 110, therein attracting the wafer to the surface 120 of the ESC. During a time at which the polarity of the clamping voltage V is reversed (*e.g.,* when the square wave clamping voltage crosses 0 volts), however, the cooling gas backpressure F_{gas}

5   may exceed the clamping force F_{esc}, and the wafer 110 may accelerate away from the surface 120 of the ESC 105. The wafer 110 may move a distance x away from the ESC 105 due to a repelling force defined by the cooling gas backpressure F_{gas}, and/or other forces, such as gravity (not shown) if the ESC is oriented upside down. The wafer 110 cannot move with an infinite velocity v,

10   however, and the movement of the wafer is limited by its inertial mass. As described by Newton's Second Law, $F = ma$, the net force F, which is the sum of the clamping force F_{esc} and the backpressure force F_{gas}, for instance, is equal to the inertial mass m of the wafer 110, multiplied by an acceleration a of the wafer, wherein the acceleration is defined as a derivative of the velocity and distance

15   *i.e., $a=dv/dt=d^2x/dt^2$.*

According to one aspect of the present invention, a position of the wafer 110 can be determined as a function of time t, wherein a minimum time dt for which the wafer will not be lost (*e.g.,* the wafer is confined to a region proximate to the ESC 105) can be determined. It should be noted that the clamping force

20   F_{esc} and cooling gas backpressure F_{gas}, for example, generally vary as the clamping voltage V crosses 0 volts, since the clamping voltage has a rise-time which is a function of time t, and the backpressure is operable to change with time as a volume of the cooling gas between the wafer 110 and the surface 120 of the ESC 105 expands or compresses.

25   Mathematically, the dynamics of the inertial confinement of the ESC can be expressed as follows. A movement of the wafer 110 will generally observe Newton's Second Law, $F = ma$, wherein F is the net force on the wafer. The net

force F, for example, can be expressed as the sum of the gas backpressure force $F_{gas}(x,t)$, and the clamping force $F_{esc}(x,t)$, wherein F is a function of distance x and time t, thereby leading to

$$F(x,t) = F_{gas}(x,t) - F_{esc}(x,t) = m\frac{d^2x}{dt^2}. \qquad (2)$$

5   Initially, when the wafer 110 is not moving, both the gas backpressure force F_{gas}, and the clamping force F_{esc} are generally constant, such that a static gas backpressure force $F_{gas}(0)$ is

$$F_{gas}(0) = \frac{P \cdot 1.013 \times 10^5 \cdot \pi \cdot R_W^2}{760}, \qquad (3)$$

where P is the gas backpressure (in Torr) applied for desired cooling of the

10   wafer, and R_W is a radius of the wafer. A static clamping force $F_{esc}(0)$ is further expressed as

$$F_{esc}(0) = \frac{\pi \cdot R_W^2 \varepsilon_0 (k \cdot V_0)^2}{2(d + k \cdot gap)^2}, \qquad (4)$$

where ε_0 is the free space permittivity (e.g., $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m), k is the dielectric constant of the insulating dielectric layer 125, d is the thickness of dielectric layer,

15   gap is the static gap length (not shown) between the surface of the ESC 105 and the surface of the wafer 110 (e.g., occupied by the cooling gas), and V_0 is the applied clamping voltage. The static gap length gap, for example, can be associated with a surface roughness of the surface 120 of the ESC 105.

When the applied single phase square wave clamping voltage V crosses 0

20   volts, for example, the wafer 110 may lose the clamping force F_{esc} and begin to move away from the surface 120 of the ESC 105, wherein the gas backpressure force F_{gas} is defined as a function of distance x and time t,

$$F_{gas}(x,t) = \frac{F_{gas}(0) \cdot gap}{x + gap}, \qquad (5)$$

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and the clamping force F_{esc} is also a function of x and t,

$$F_{esc}(x,t) = \frac{\pi \cdot R_W{}^2 \varepsilon_0 (k \cdot V(t))^2}{2(d + k \cdot (x + gap))^2},$$ (6)

where $V(t)$ is a clamping voltage across the wafer 105 and an electrode 140 associated with the ESC 105. Alternatively, $V(t)$ is a clamping voltage between 5 two or more electrodes 140 associated with the ESC 105. Furthermore, $V(t)$, for example, is no longer constant and will vary exponentially according to an RC time constant associated with the system 100, where R is the resistance of the wafer 105 and C is the capacitance between the wafer and the electrode 140.

Therefore, the clamping voltage $V(t)$ can be expressed as follows:

10 $$V(t) = V_0 \left(1 - 2 \cdot \exp\left(\frac{-t}{RC}\right) \right).$$ (7)

Combining equations (5) and (6) into equation (2), the dynamics of the inertial confinement of the wafer 110 can be expressed as a differential equation

$$D(x,t) = \frac{d^2 x}{dt^2} = \frac{1}{m} \cdot \left(\frac{F_{gas}(0) \cdot gap}{x + gap} - \frac{\pi \cdot R_W{}^2 \varepsilon_0 \left(k \cdot V_0 \left(1 - 2 \cdot \exp\left(\frac{-t}{RC}\right) \right) \right)^2}{2(d + k \cdot (x + gap))^2} \right).$$ (8)

The differential equation (8) can be solved numerically for the position $x(t)$ 15 of the wafer 110 by using a computerized differential equation solver, such as Mathcad produced by Mathsoft Engineering and Education, Inc., for a typical 150 mm wafer. After the position $x(t)$ is obtained, the velocity $v(t) = dx/dt$, and the acceleration $a(t) = d^2x/dt^2$ can further be derived.

Figs. 2A-2D illustrate an exemplary single-phase square wave clamping 20 voltage V which is applied to a classic flat-plate ESC 105 of Fig. 1. By controlling parameters such as rise-time, pulse width, and pulse repetition frequency (prf) of the single-phase square wave AC clamping voltage signal, the wafer 110 can be

reliably clamped due, at least in part, to the wafer inertial mass during voltage switching. Fig. 2A, for example, illustrates an applied clamping voltage V_0 and the voltage $V(t)$ across the wafer 105 and electrode 140 of Fig. 1. The exemplary square wave clamping voltage V of Fig. 2A generally defines the clamping force

5   F_{esc}, and Fig. 2B illustrates a result of solving for $x(t)$, wherein a maximum x (e.g., the maximum distance which the wafer moves) and a time required for x to return back to 0 (e.g., an initial position of the wafer) can be determined. The elapsed time between when the wafer leaves and returns to its initial position, for example, is termed the wafer impact time. Figures 2C and 2D illustrate the

10   velocity $v(t)$ and acceleration $a(t)$ of the wafer, respectively, and are illustrated for reference.

As an example, the graphs of Figs. 2A-2D utilize a flat-plate ESC 105 of Fig. 1 having a 150 mm diameter and a 0.2 mm insulative dielectric layer 125 (e.g., an alumina layer) is utilized, wherein a gap of approximately 3 μm between

15   the wafer 110 and the ESC 105 is maintained with a gas backpressure P of approximately 200 Torr. A clamping voltage V of approximately ±2000 volts is applied, wherein a static clamping force of approximately 250 Torr is provided. The capacitance C is approximately 3.4 nF, the resistance R is approximately 20 Ω, therein defining the RC time constant as $RC = 6.8 \times 10^{-8}$ seconds.

20   According to another exemplary aspect of the invention, a MEMS-based ESC 105 of Fig. 1 may also be utilized in accordance with the present invention. Fig. 3 illustrates a plan view of an exemplary MEMS-based ESC 150, wherein a surface 155 of the ESC comprises a plurality of microstructures 160. The plurality of microstructures 160, for example, are operable to generally maintain a

25   consistent gap between the wafer (not shown) and the surface 155 of the ESC 150. Again, by controlling parameters such as rise-time, pulse width, and pulse repetition frequency of the single-phase square wave AC voltage signal, the

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wafer can be reliably clamped due, at least in part, to the wafer inertial mass during voltage switching. Utilizing a MEMS-based ESC 150, however, generally permits the clamping voltage V to be significantly lower than the classic flat-plate ESC 105 of Fig. 1.

5   The graphs illustrated in Figs. 4A-4D, for example, depict exemplary waveforms of clamping voltage V, wafer position x, velocity v, and acceleration a, respectively, as a function of time for a MEMS-based ESC 150 of Fig. 3 according to the present invention. For example, a MEMS-based ESC 150 having a 150 mm diameter is utilized, wherein a *gap* of approximately 1 μm

10   between the wafer (not shown) and the ESC is maintained with a backpressure P of approximately 200 Torr, and a clamping voltage V of approximately ±112 volts, therein providing approximately 400 Torr static clamping force. The capacitance C, for example, is approximately 78.2 nF, the resistance R is approximately 20 Ω, therein defining the RC time constant of $RC = 1.56 \times 10^{-6}$ seconds.

15   Referring again to Figs. 2A and 4A, according to another exemplary aspect of the present invention, the pulse width of the clamping voltage V can have a generally large range. A lower limit of the pulse width, for example, is preferably longer than the wafer impact time as described above. Furthermore, in another example, the pulse width is preferably greater than 10 times the wafer

20   impact time in order to provide a higher reliability factor for the ESC. For example, the shortest pulse widths for the classic and MEMS-based ESCs described above are approximately 1.3 μsec and 11 μsec, respectively. An upper limit of the pulse width, for example, is determined by a predetermined declamping time associated with a throughput specification for the ESC, since

25   the declamping time is proportional to the clamping time under a particular clamping voltage. If a declamping time shorter than 0.5 seconds is desired, for example, a range of the pulse width for the above classic ESC example should

be from approximately 1.3 μsec to approximately 0.5 seconds, corresponding to

pulse repetition frequencies of approximately 300 kHz to 1 Hz. A range of the

pulse width according to the above MEMS-based ESC example should be

approximately between 11 μsec to 0.5 seconds, corresponding to a prf of

5   approximately 40 kHz to 1 Hz.

According to another exemplary aspect of the present invention, there

exists no tight limit for the RC constant associated with the system 100 of Fig. 1.

For example, R is the resistance of a silicon wafer, and can be generally varied in

a mild range. For the MEMS-based ESC 150 of Fig. 3, for example, the

10   capacitance C is directly determined by the gap between surface 155 and the

wafer (not shown), wherein the clamping force F_{esc} is furthermore directly

determined by the gap. For a classic flat-plate ESC, however, both the

capacitance C and the clamping force F_{esc} are generally determined by a

combination of the gap and the dielectric layer 125 of Fig. 1. According to one

15   example, an RC time constant should be maintained as small as possible,

however, the RC time constant is generally limited by the resistance R of the

wafer and chuck surface conditions. Generally, the shorter the RC time constant,

the smaller the movement x of the wafer, and the shorter the wafer impact time.

Similarly, the larger the RC time constant, the larger the movement x of the

20   wafer, and the larger the wafer impact time. If the RC time constant is too large,

for example, the wafer 110 may move a distance ($e.g.$, an "escape distance") so

far away from the ESC 105 that it cannot be retrieved by electrostatic force,

wherein the wafer is subsequently "lost" from the ESC. According to another

example, the RC time constant will affect the rise time of the single-phase square

25   wave clamping voltage.

As can be seen through the above examples, the classic flat-plate ESC is

generally more forgiving, wherein a wafer movement x of 7×10^{-10} m (0.0007 μm)

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and a 1.2×10^{-6} second wafer impact time is exhibited when the clamping voltage V switches polarity and crosses 0 volts. This distance can be considered negligible when compared to the 3 μm averaged static *gap*. The MEMS-based ESC example is relatively less forgiving, with a 1×10^{-7} m (0.1 μm) wafer

5   movement x and a 1.2×10^{-5} second wafer impact time due to the capacitance C being approximately one order of magnitude larger. However, an advantage of the MEMS-based ESC over the classic ESC is that the *gap* between the ESC and the wafer can be well controlled in the MEMS-based ESC, so that a smaller *gap* and a lower clamping voltage V (or a larger clamping force under the same

10   voltage) is possible. A lower clamping voltage V, for example, lowers a risk of a deleterious electrical discharge, and also lowers a risk of forming particulates which may contaminate the ESC.

According to another example, an upper limit of the RC time constant is such that the wafer movement x is less than one tenth of the initial *gap*, since the

15   *gap*, for example, has a large impact on the gas cooling capability. However, since the pulse width can vary by a large range, a longer pulse width (lower pulse repetition frequency) can be selected in order to minimize the impact of the wafer movement. Preferably, the pulse width is less than 0.1 seconds, and the rise-time of the square wave clamping voltage is less than 2 μsec, for a maximum

20   movement x of approximately 0.5 μm and 0.11 μm for the classic ESC and MEMS-based ESC, respectively. While the pulse width is not critical, a 0.1 msec to 0.1 second prf will provide a generally rapid de-clamping time.

In accordance with the another exemplary aspect of the present invention, the ESCs of Figs. 1 and 3 may further comprise electrode patterns of various

25   types, including, for example, a simple uni-polar structure for a plasma-environment system or a simple D-shape bi-polar structure for a vacuum-environment system. Furthermore, the present invention does not require

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complicated electrode patterns or complex signal timing control electronics. The wafer can be almost instantaneously de-clamped after the clamping voltage V is turned off, due, at least in part, to the pulse width during clamping being short enough to significantly prevent charge migration and accumulation to the

5   dielectric front surface and/or back surface of the wafer.

While exemplary methods are illustrated and described herein as a series of acts or events, it will be appreciated that the present invention is not limited by the illustrated ordering of such acts or events, as some steps may occur in different orders and/or concurrently with other steps apart from that shown and

10   described herein, in accordance with the invention. In addition, not all illustrated steps may be required to implement a methodology in accordance with the present invention. Moreover, it will be appreciated that the methods may be implemented in association with the systems illustrated and described herein as well as in association with other systems not illustrated.

15   Referring now to Fig. 5, a method 200 for clamping a semiconductor wafer to an electrostatic chuck is illustrated in accordance with one exemplary aspect of the present invention. Beginning with act 205, a single-phase square wave clamping voltage is determined, based, at least in part, on an inertial response time of the wafer. In act 210, the wafer is placed on a clamping surface of the

20   electrostatic chuck. The clamping surface, for example, may comprise a flat-plate electrostatic chuck surface, or a MEMS-based electrostatic chuck surface comprising a plurality of microstructures extending from the chuck surface. In act 215, the determined single-phase square wave clamping voltage is applied to the ESC, wherein the wafer is generally clamped to the ESC. The determined

25   clamping voltage, for example, is operable to generally induce an electrostatic force between the ESC and the wafer, therein generally attracting the wafer to the surface of the ESC. In act 220, the single-phase square wave clamping

voltage is stopped, therein de-clamping the wafer from the ESC. The de-clamping time, for example, is minimized due to the clamping voltage determination performed in act 205.

Although the invention has been shown and described with respect to a certain preferred embodiment or embodiments, it is obvious that equivalent alterations and modifications will occur to others skilled in the art upon the reading and understanding of this specification and the annexed drawings. In particular regard to the various functions performed by the above described components (assemblies, devices, circuits, etc.), the terms (including a reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component which performs the specified function of the described component (*i.e.*, that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein illustrated exemplary embodiments of the invention. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several embodiments, such feature may be combined with one or more other features of the other embodiments as may be desired and advantageous for any given or particular application.